FIG.1

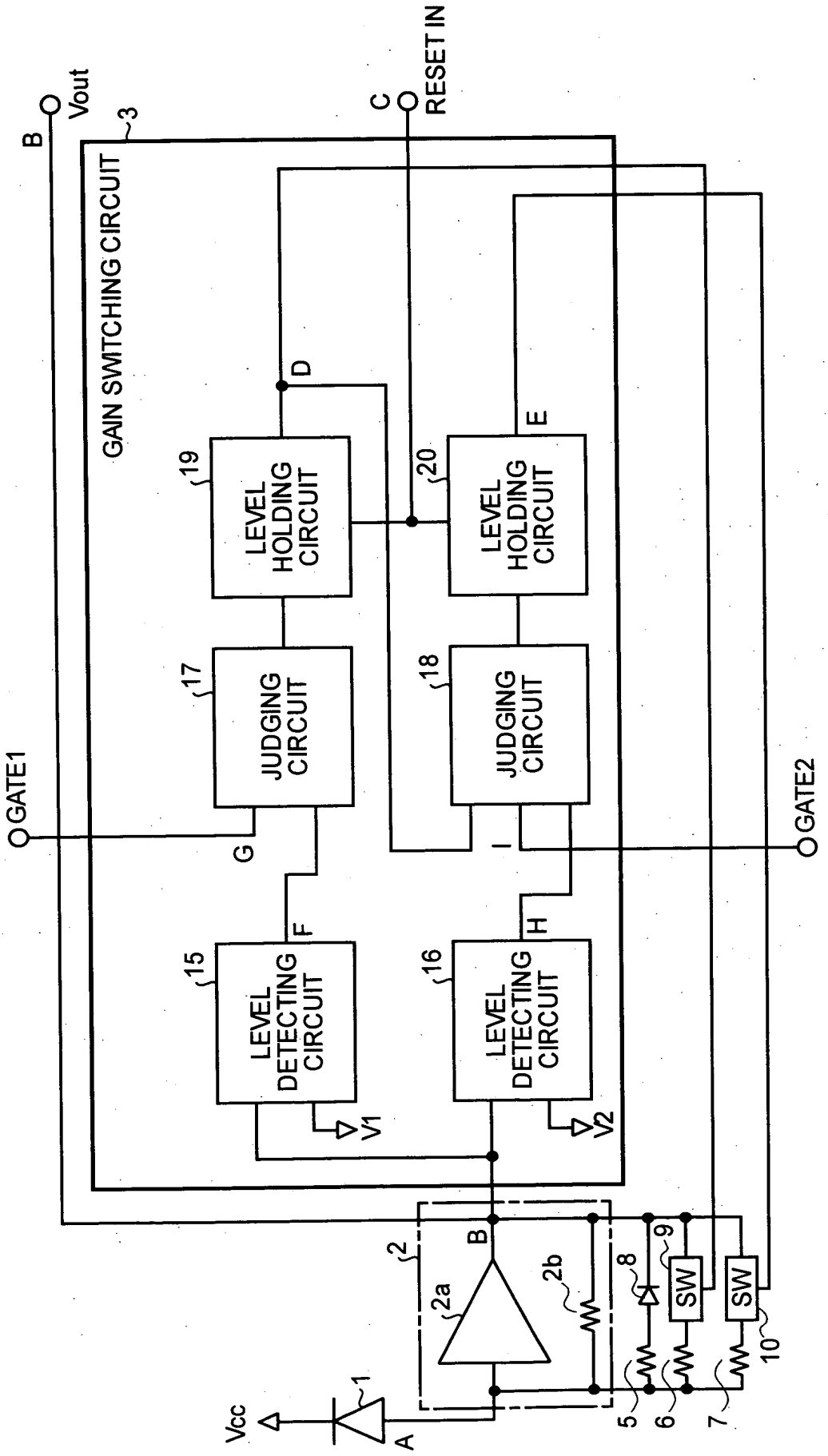

Vout
B
3
GAIN SWITCHING CIRCUIT
C
RESET IN
D
E
19
LEVEL HOLDING CIRCUIT
20
LEVEL HOLDING CIRCUIT
17
JUDGING CIRCUIT
18
JUDGING CIRCUIT
GATE1
G
I
GATE2
F
H
15
LEVEL DETECTING CIRCUIT
16
LEVEL DETECTING CIRCUIT
V1
V2
2
B
2a
2b
8
9
SW
SW
10
Vcc
1
A
5
6
7

FIG.2

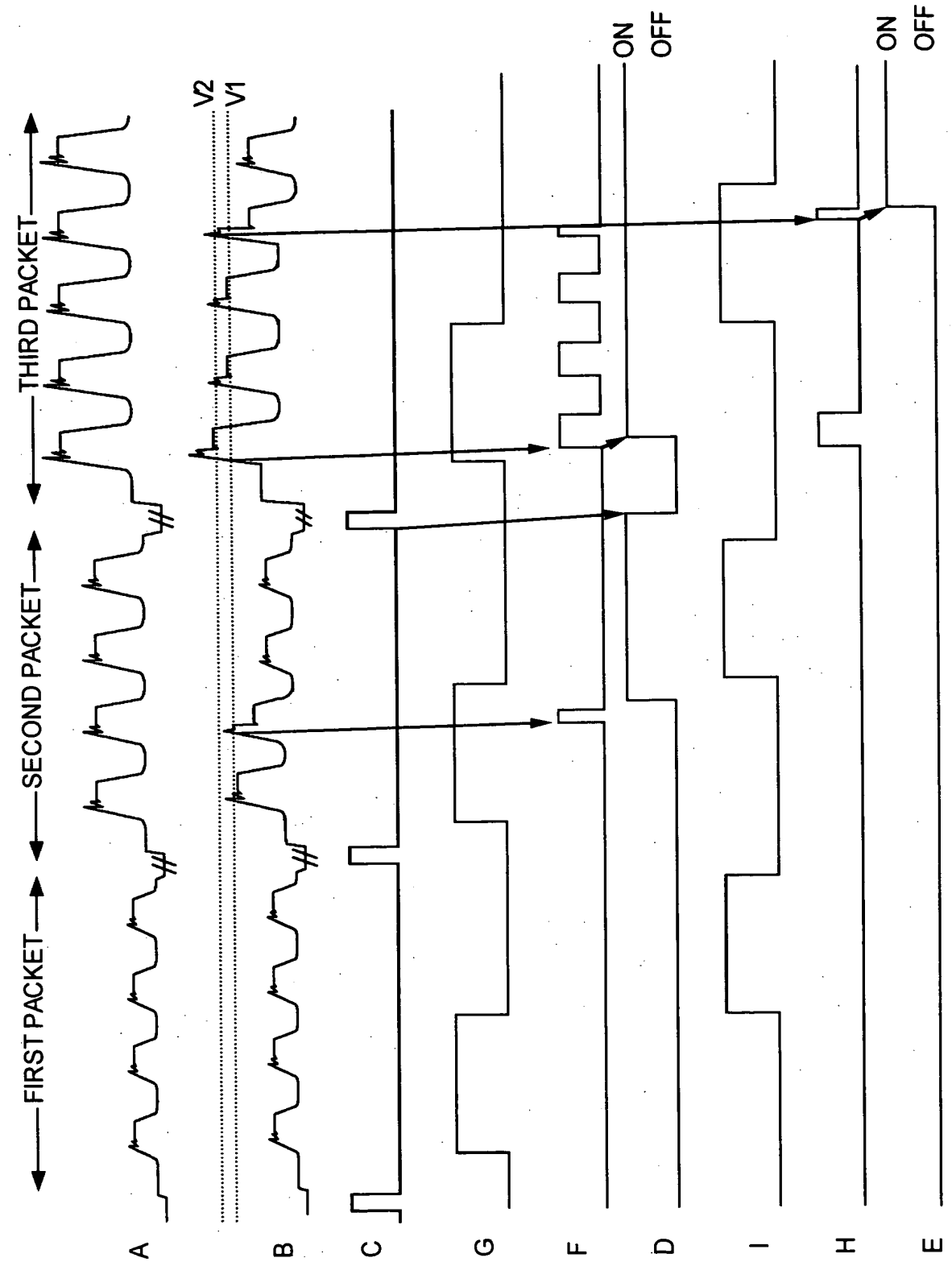

FIRST PACKET
SECOND PACKET
THIRD PACKET
V2
V1
ON
OFF
ON
OFF
A
B
C
G
F
D
I
H
E

FIG.3

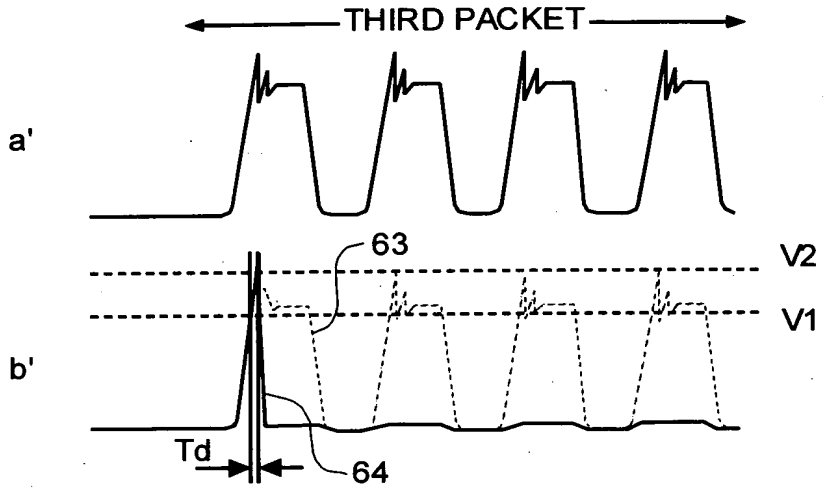


FIG.4

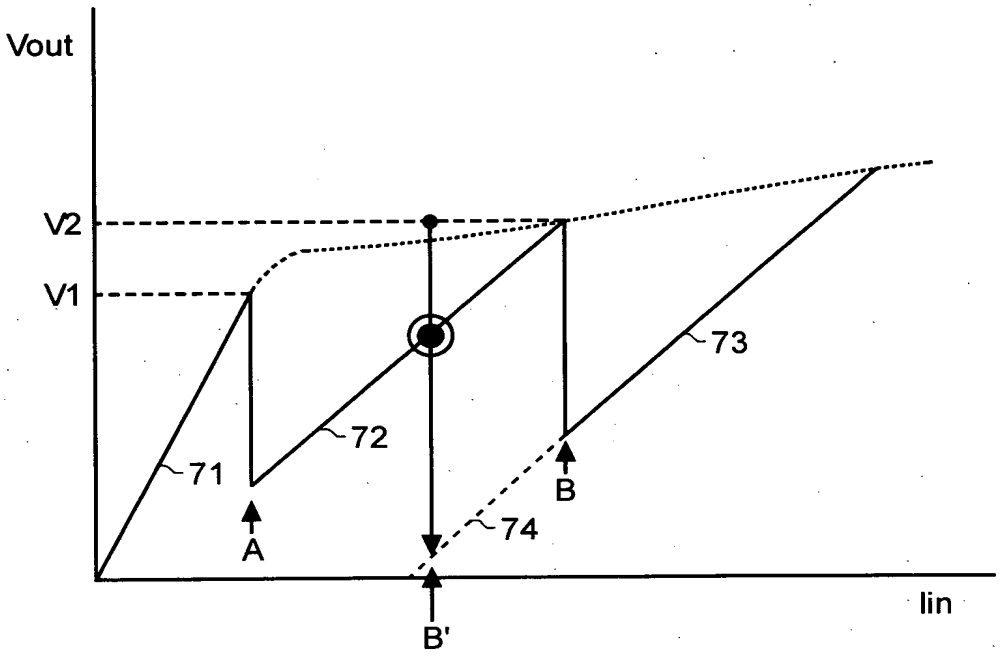


FIG.5

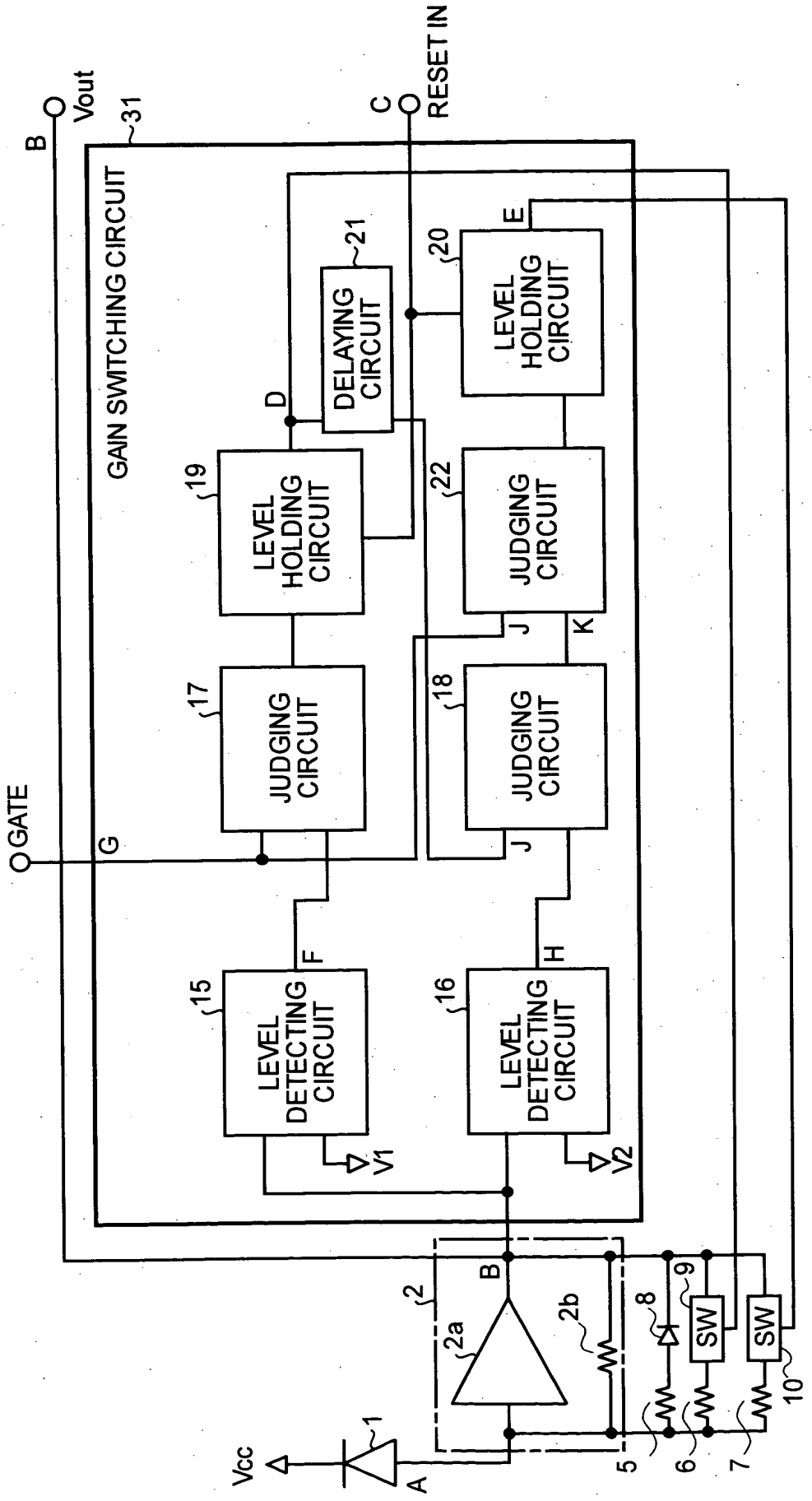
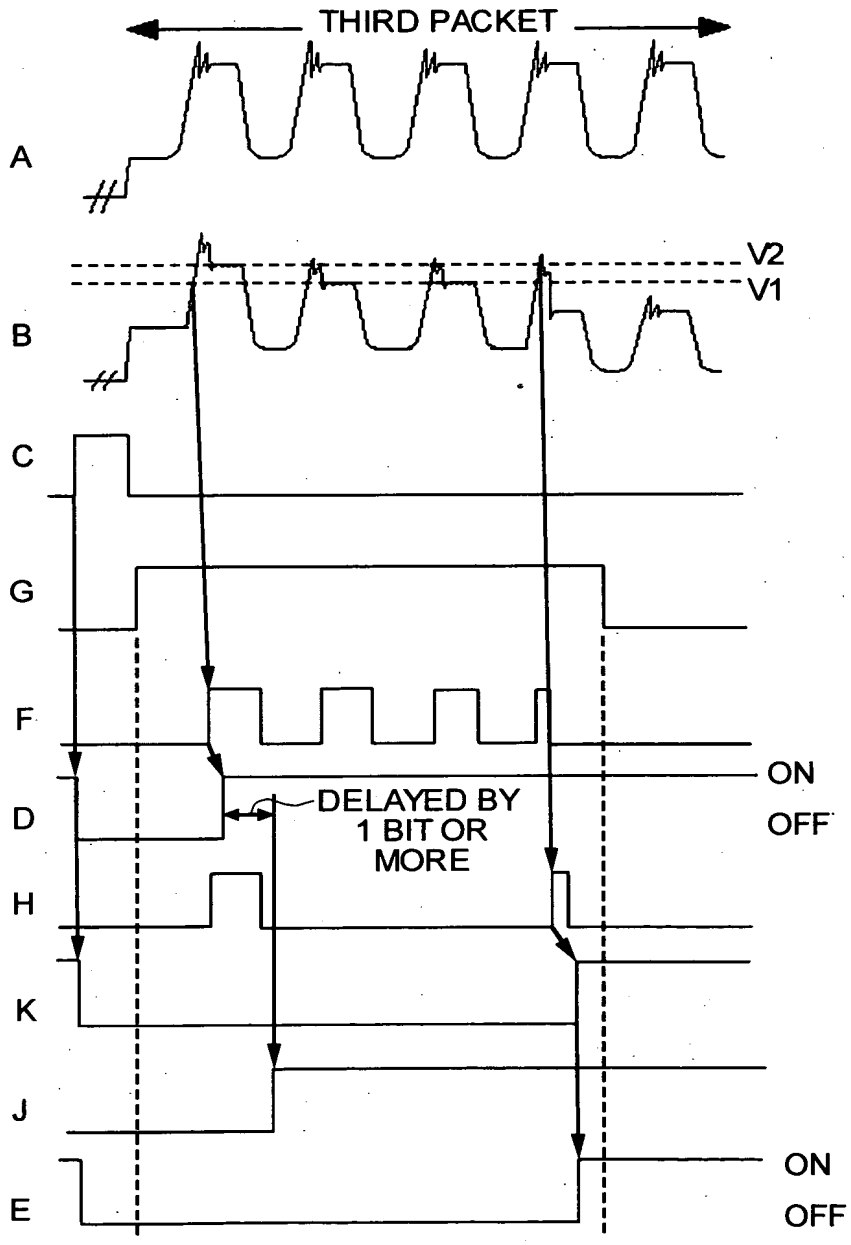

Vout
B
31
GAIN SWITCHING CIRCUIT
RESET IN
C
E
21
DELAYING CIRCUIT
20
LEVEL HOLDING CIRCUIT
D
19
LEVEL HOLDING CIRCUIT
22
JUDGING CIRCUIT
J
K
17
JUDGING CIRCUIT
18
JUDGING CIRCUIT
GATE
G
J
F
H
15
LEVEL DETECTING CIRCUIT
16
LEVEL DETECTING CIRCUIT
V1
V2
2
B
2a
2b
8
9
SW
SW
10
Vcc
1
A
5
6
7

FIG.6


THIRD PACKET
A
B
V2
V1
C
G
F
D
DELAYED BY
1 BIT OR
MORE
ON
OFF
H
K
J
E
ON
OFF

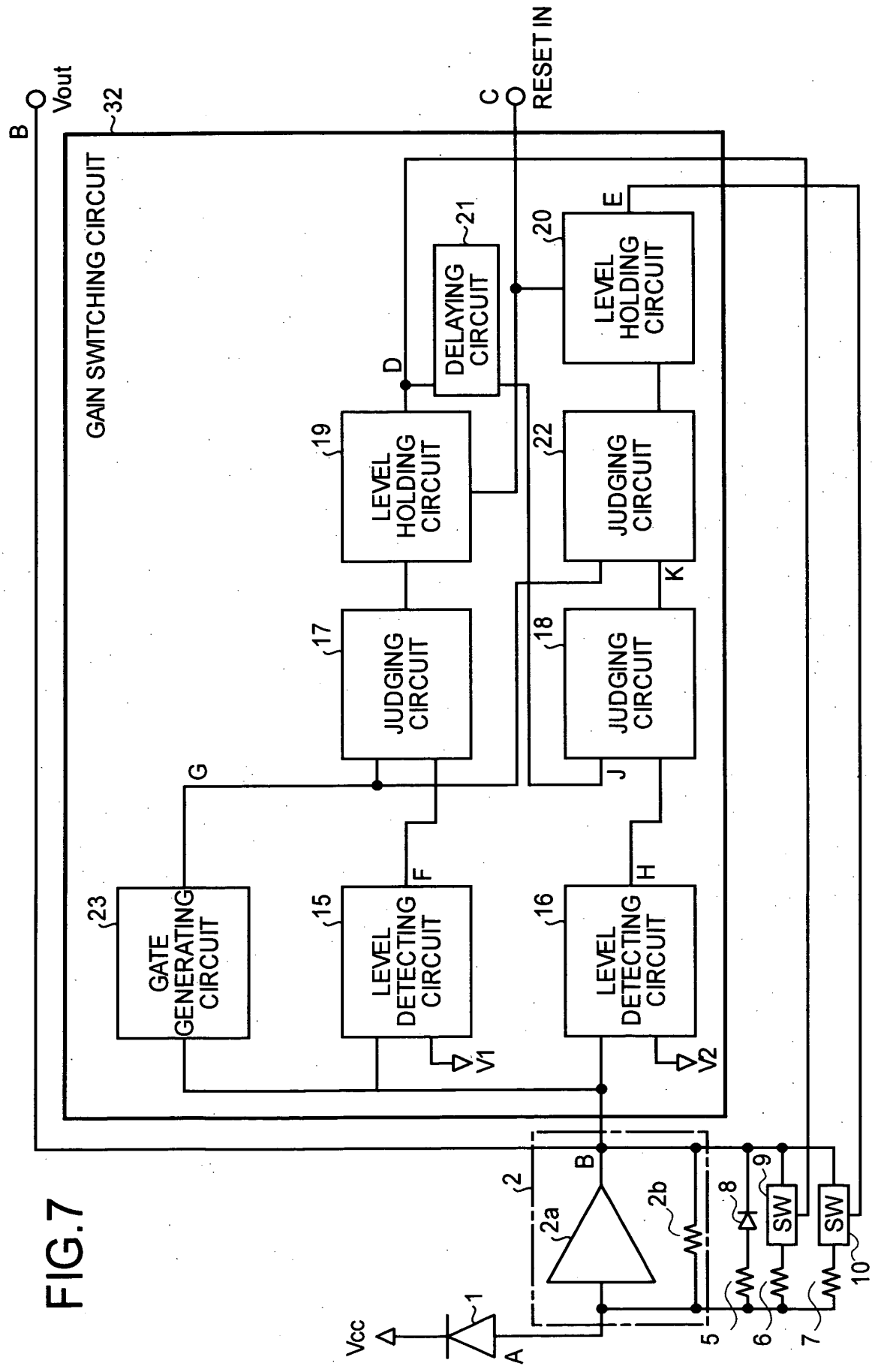

B
Vout
32
GAIN SWITCHING CIRCUIT
C
RESET IN
21
DELAYING CIRCUIT
20
E
LEVEL HOLDING CIRCUIT
D
19
LEVEL HOLDING CIRCUIT
22
JUDGING CIRCUIT
K
17
JUDGING CIRCUIT
18
JUDGING CIRCUIT
J
G
23
GATE GENERATING CIRCUIT
15
LEVEL DETECTING CIRCUIT
F
16
LEVEL DETECTING CIRCUIT
H
V1
V2
2
B
2a
2b
8
9
SW
SW
10
Vcc
1
A
5
6
7

FIG.7

FIG.8

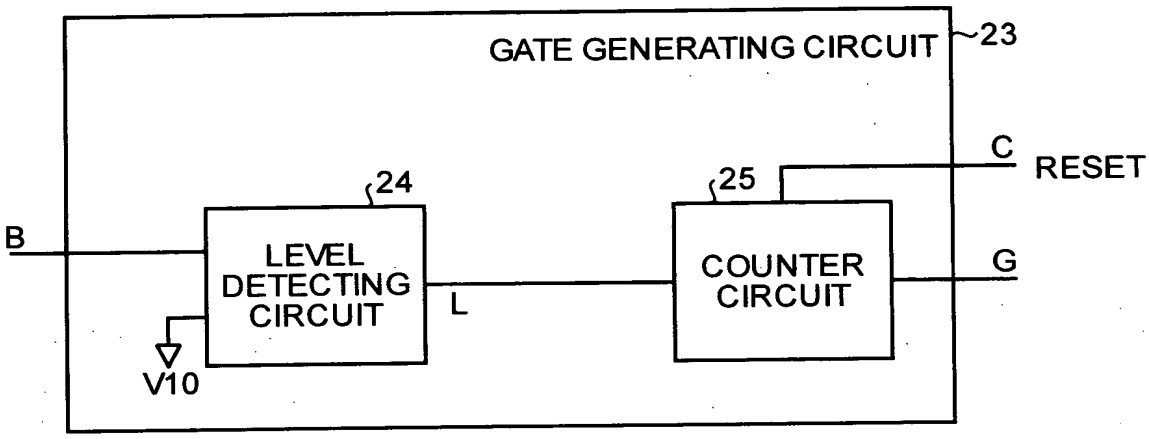

GATE GENERATING CIRCUIT
23
C
RESET
24
25
B
LEVEL DETECTING CIRCUIT
L
COUNTER CIRCUIT
G
V10

FIG.9

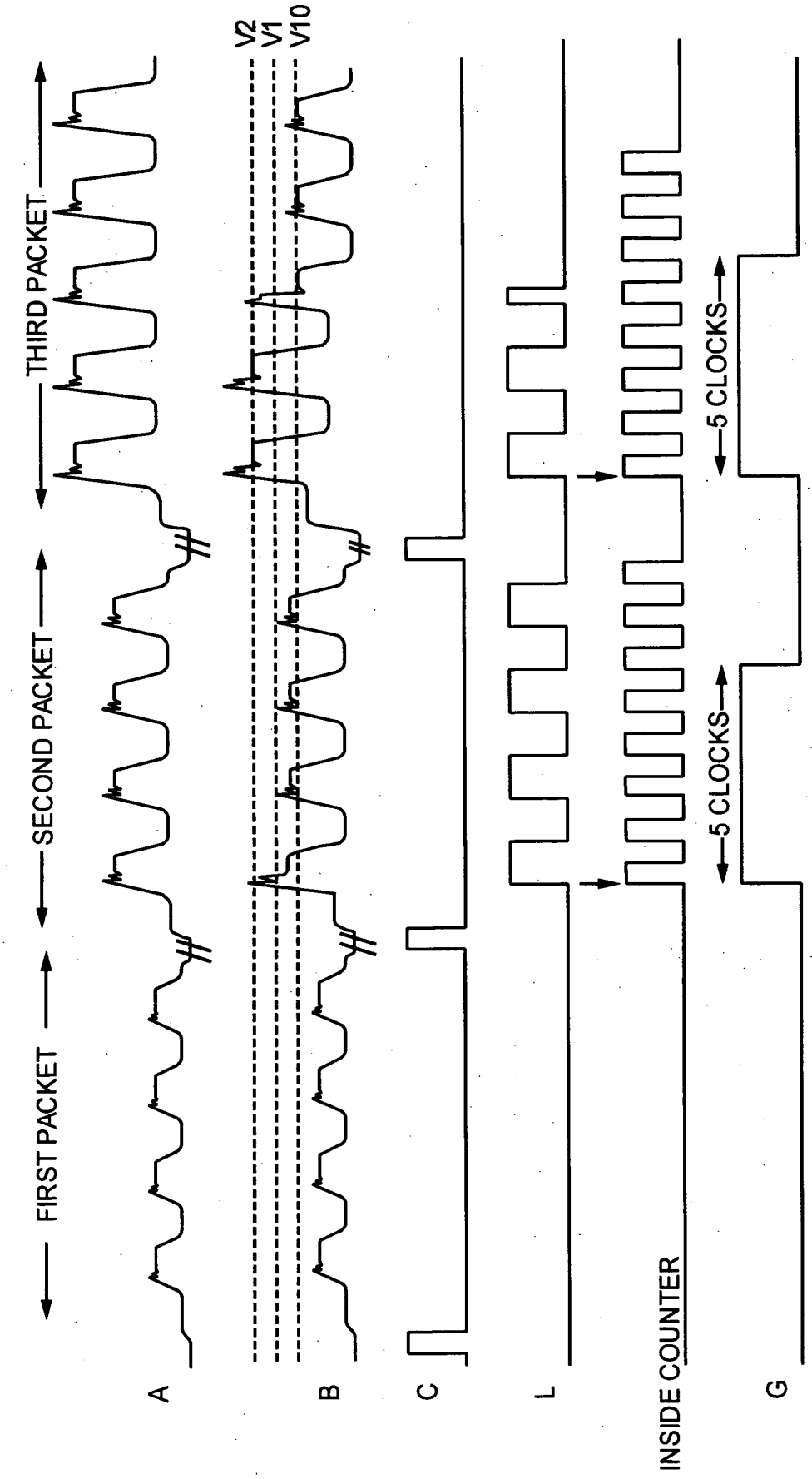

FIRST PACKET
SECOND PACKET
THIRD PACKET
V2
V1
V10
A
B
C
L
INSIDE COUNTER
5 CLOCKS
5 CLOCKS
G

FIG.10

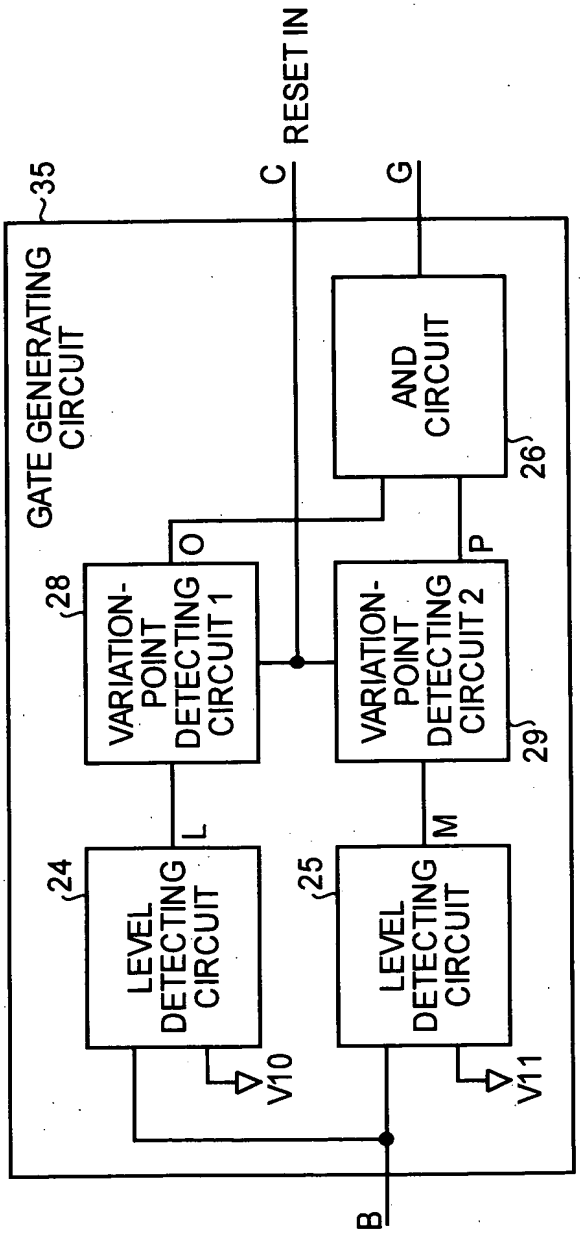
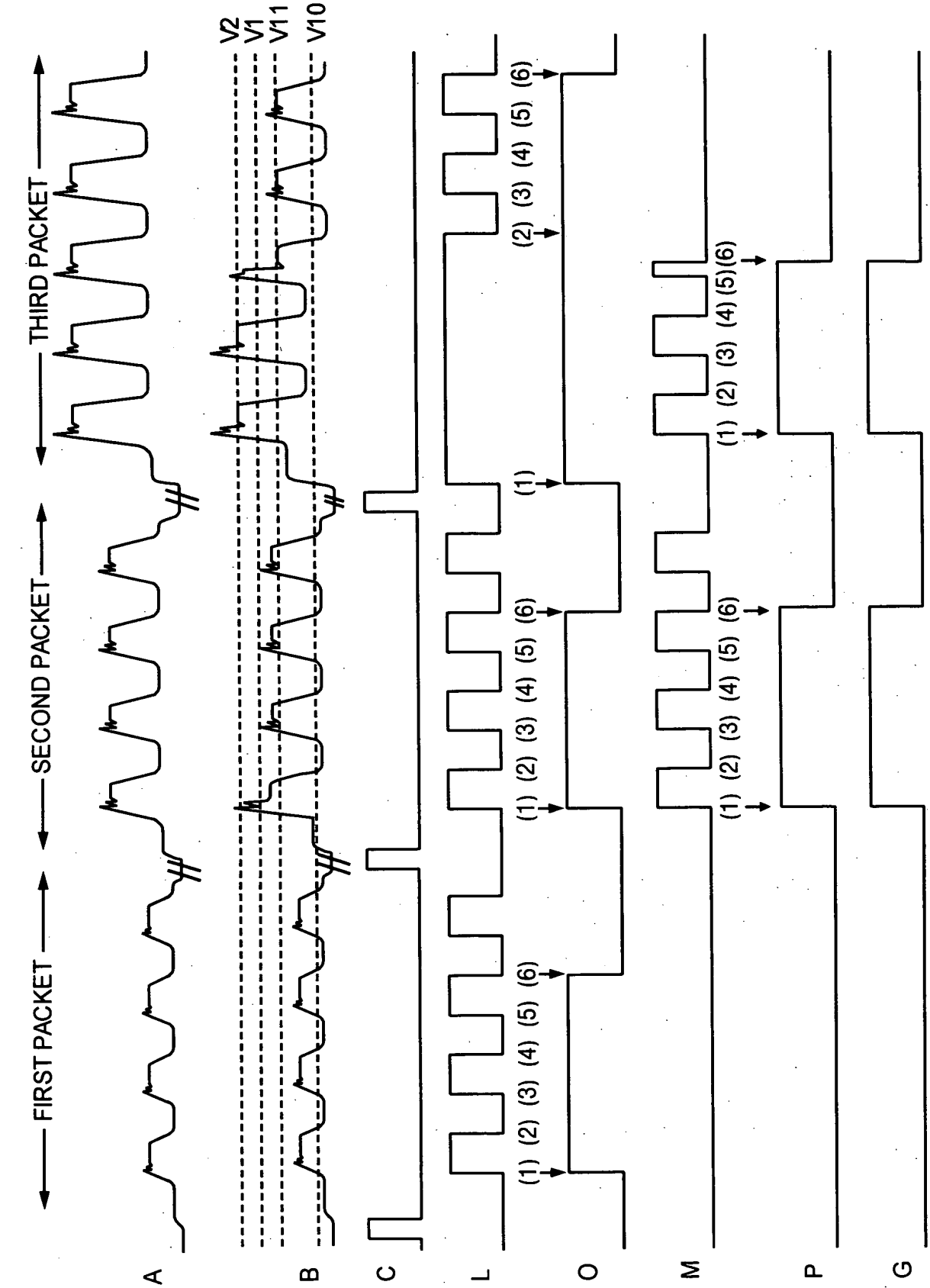

35
GATE GENERATING CIRCUIT
C
RESET IN
G
AND CIRCUIT
26
O
P
28
VARIATION-POINT DETECTING CIRCUIT 1
VARIATION-POINT DETECTING CIRCUIT 2
29
L
M
24
LEVEL DETECTING CIRCUIT
25
LEVEL DETECTING CIRCUIT
V10
V11
B

FIG.11


FIRST PACKET
SECOND PACKET
THIRD PACKET
V2
V1
V11
V10
A
B
C
L
O
M
P
G
(1) (2) (3) (4) (5) (6)